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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,793	01/18/2002	Akihiko Ebina	15.55.6364	9576

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/050,793	Applicant(s) EBINA, AKIHIKO
	Examiner Thomas L Dickey	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *16-22* is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II, claims 1-15 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 01/18/02 is acceptable.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations that the first body region of the second conduction type is electrically connected to the source region of the first conduction type, the first body region of the second conduction type is electrically connected to the first base region of the second conduction type, the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, the first body region of the first conduction type is electrically connected to the second collector region

of the first conduction type, the source region of the second conduction type is electrically connected to the second collector region of the first conduction type, the drain region of the second conduction type is electrically connected to the second base region of the second conduction type, the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and the first gate electrode layer is electrically connected to the second gate electrode layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. The applicant should consider that each of these connections appears in the same claim and thus must appear in the same drawing. Many applicants find circuit diagrams helpful in showing electrical connections when more than two or three such connections are claimed.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over WOLF "Silicon Processing for the VLSI Era" in view of Zheng et al. " SOI bipolar-MOS merged transistors for BiCMOS application," and SCHWANK et al. (6,268,630).

Wolf discloses a semiconducting device with a semiconductor layer, an element isolation region formed in the semiconductor layer; and a first element forming region and a second element forming region defined by the element isolation region; wherein the first element forming region includes both a first bi-polar transistor Q1 and a first field effect transistor M1; the first bi-polar transistor Q1 includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type, the first field effect transistor M1 includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the

first conduction type, the first field effect transistor M1 further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type, the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and wherein the second element forming region includes both a second bi-polar transistor Q2 and a second field effect transistor M2, the second bi-polar transistor Q2 includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type, the second field effect transistor M2 includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type, the second field effect transistor M2 further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type, the source region of the second conduction type is electrically connected to the second collector region of the first conduction type, the drain region of the second conduction type is electrically connected to the second base region of the second conduction type, the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and the first gate electrode layer is electrically connected to the second gate electrode layer. Note figures 7-74(a) (top figure. Note that this figure includes two extra MOSFETS that are not

needed to meet the claim) and 7-75(a) of Wolf. Wolf does not disclose an insulation layer upon which the semiconductor layer is formed, or electrically connecting the first body region of the second conduction type to the first base region of the second conduction type, or electrically connecting the first body region of the second conduction type to the source region of the first conduction type, or electrically connecting the first body region of the first conduction type to the second collector region of the first conduction type. Wolf does, however, teach electrically connecting the source region of the first conduction type to the first base region of the second conduction type (as opposed to electrically connecting both of these regions to the first body region of the second conduction type), and naturally, as stated above as a claim limitation, Wolf teaches that the source region of the second conduction type is electrically connected to the second collector region of the first conduction type.

However, Zheng et al. discloses a complementary BiCMOS device formed in a semiconductor layer formed on an insulation layer. Note figure 1 of Zheng et al. Further, Schwank et al. discloses an SOI CMOS transistor wherein on the right side, the first body region 28 of the second conduction type is electrically connected to the source region 52 of the first conduction type by way of body tie 56 and electrode 58, and wherein on the left side, the first body region 28 of the first conduction type is electrically connected to the source region 52 of the second conduction type by way of the other body tie 56 and the other electrode 58. Note figure 1 of Schwank et al. Therefore, it would have been obvious to a person having skill in the art to augment Wolf's semiconducting

device with the insulation layer upon which the semiconductor layer is formed such as taught by Zheng et al. in order to increase the transconductance to thus provide faster response and higher frequency operation, and to augment the semiconducting device by electrically connecting the first body region of the second conduction type to the source region of the first conduction type and thus to the first base region of the second conduction type, and electrically connecting the first body region of the first conduction type to the source region of the second conduction type, and thus to the second collector region of the first conduction type, such as taught by Schwank et al., in order to harden the device against SEU radiation.

Allowable Subject Matter

7. Claim 15 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising an insulation layer, a semiconductor layer formed on the insulation layer, an element isolation region formed in the semiconductor layer, and a first element forming region and a second element forming region defined by the element isolation region, where the first element forming region includes both a first bi-polar transistor and a first field effect transistor, a first gate electrode layer is formed on the semiconductor layer, the first gate electrode layer is formed in a manner to cross over the first element forming region, a first electrode layer is formed on the semiconductor layer, the first electrode layer has one end section continuing to a side section of the first gate

electrode layer, and another end section reaching the element isolation region, a first impurity diffusion layer of a first conduction type is formed at least in a part of a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer and the element isolation region, a second impurity diffusion layer of the first conduction type is formed in a second region surrounded by the first gate electrode layer and the element isolation region, a third impurity diffusion layer of the first conduction type is formed in a third region defined by the first gate electrode layer in a forming region of the first bi-polar transistor , the first electrode layer and the element isolation region, a first body region of a second conduction type is formed below the first gate electrode layer in a forming region of the first field effect transistor and the first electrode layer, a first impurity diffusion layer of the second conduction type is formed below the first gate electrode layer in the forming region of the first bi-polar transistor and the first electrode layer and along a periphery of the third impurity diffusion layer of the first conduction type, the first body region of the second conduction type is electrically connected to the first impurity diffusion layer of the first conduction type, and the first body region of the second conduction type is electrically connected to the first impurity diffusion layer of the second conduction type, wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor, a second gate electrode layer is formed on the semiconductor layer, the second gate electrode layer is formed in a manner to cross over the second element forming region, a second electrode layer is formed on the semiconductor layer,

the second electrode layer has one end section continuing to a side section of the second gate electrode layer, and another end section reaching the element isolation region, a second impurity diffusion layer of the second conduction type is formed in a fourth region surrounded by the second gate electrode layer in a forming region of the second field effect transistor, the first electrode layer and the element isolation region, a third impurity diffusion layer of the second conduction type is formed in a fifth region surrounded by the second gate electrode layer and the element isolation region and in the forming region of the second field effect transistor, a fourth impurity diffusion layer of the first conduction type is formed in a fifth region in a forming region of the second bi-polar transistor, a fifth impurity diffusion layer of the first conduction type is formed in a sixth region surrounded by the second gate electrode layer in the forming region of the second bi-polar transistor and the element isolation region, a body region of the first conduction type is formed below the second gate electrode layer, a fourth impurity diffusion layer of the second conduction type is formed below the second gate electrode layer in the forming region of the second bi-polar transistor and the second electrode layer and along a periphery of the fifth impurity diffusion layer of the first conduction type, the body region of the first conduction type is electrically connected to the fourth impurity diffusion layer of the first conduction type, the third impurity diffusion layer of the second conduction type is electrically connected to the fourth impurity diffusion layer of the first conduction type, the second impurity diffusion layer of the second conduction type is electrically connected to the fourth impurity diffusion layer of the second conduction type, the sec-

ond impurity diffusion layer of the first conduction type is electrically connected to the fifth impurity diffusion layer of the first conduction type, and the first gate electrode layer is electrically connected to the second gate electrode layer.

8. Claims 2-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9319 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
11/2002